REMARKS

Claims 1-3, 6-19, and 22-40 were examined and reported in the Office Action. Claims 1-3, 6-19, and 22-40 are rejected. Claims 8, 15, 23, 28, 34 and 40 are canceled. Claims 1, 10, 17, 24, 29 and 36 are amended. Claims 1-3, 6-7, 9-14, 16-19, 22, 24-27, 29-33 and 35-39 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 102(e)

It is asserted in the Office Action that claims 1-3, 6-19, and 22-40 are rejected under 35 U.S.C. § 102(e), as being unpatentable by U. S. Patent No. 6,492,835 issued to Shau ("Shau"). Applicant respectfully traverses the aforementioned rejections for the following reasons.

According to MPEP §2131, "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 1 contains the limitations of "...determining an optimum splitting variable for dividing a programmable logic array (PLA) into at least two sub-PLAs by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a

second sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; dividing a set of equations representing a PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein an OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA."

Applicant's amended claim 10 contains the limitations of "...determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing at least two sub-PLAs by avoiding unbalanced columns in an AND plane of the equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the equations representing the PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a second sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; dividing the set of equations representing the PLA into equations representing the at least two sub-PLAs; merging outputs of the equations representing the at least two sub-PLAs; determining a topological circuit representation of the equations representing the at least two sub-PLAs; applying gating logic to the topological circuit representation of the at least two sub-PLAs; and controlling power consumption in the topological representation of the

at least two sub-PLAs so only one of the at least two sub-PLAs contributes to power consumption, wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA."

Applicant's amended claim 17 contains the limitations of "...determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, said first sub-PLA and said second sub-PLA each have an AND plane and an OR plane, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; divide the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determine a topological circuit representation of first sub-PLA and the second sub-PLA; apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein the topological circuit representation an OR plane of the first sub-PLA is interleaved with an OR plane of the second sub-PLA."

Applicant's amended claim 24 contains the limitations of "...determine an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing at least two sub-PLAs by avoiding unbalanced columns in an AND plane of the equations representing the sub-PLA and selecting a column with smallest overhead in the AND plane of the equations representing the sub-PLA, each sub-PLA of said at least two sub-PLAs having an AND plane and an OR plane, a first sub-PLA of said at least two sub-PLAs includes products in which said splitting variable is in complemented form, a second sub-PLA of said at

least two sub-PLAs includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; divide the set of equations representing the PLA into equations representing the at least two sub-PLAs; merge outputs of the equations representing the at least two sub-PLAs; determine a topological circuit representation of the equations representing the at least two sub-PLAs; apply gating logic to the topological circuit representation of the at least two sub-PLAs; and control power consumption in the topological circuit representation of the at least two sub-PLAs so only one of the at least two sub-PLAs contributes to power consumption, wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA."

Applicant's amended claim 29 contains the limitations of "...determining an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an AND plane and an OR plane by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA; dividing the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA

contributes to power consumption, wherein an OR plane of the topological circuit representation of the first sub-PLA is separated from an OR plane of the topological circuit representation of the second sub-PLA."

Applicant's amended claim 36 contains the limitations of "...determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an AND plane and an OR plane by avoiding unbalanced columns in an AND plane of a set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA, the first sub-PLA includes products in which said splitting variable is in complemented form, the second sub-PLA includes products in which said splitting variable is in uncomplemented form, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA; divide a set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determine a topological circuit representation of the first sub-PLA and the second sub-PLA; apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein in the topological circuit representation an OR plane of the first sub-PLA is separated from an OR plane of the second sub-PLA."

It is asserted in the Office Action that Shau teaches "determining an optimum splitting variable for dividing a programmable logic array (PLA)" based on the disclosure at column 4, lines 31-33. This portion of Shau, however, does not teach, disclose or suggest a "splitting variable." Shau does disclose optimization methods, but not by using an optimum splitting variable. Shau teaches using miniterm sorting procedures, before a PLA is split into sub-PLAs (see Shau, column 7, line 15 to column 8, line 26). Nowhere in Shau is it taught, disclose or suggested to "determining an optimum splitting variable for dividing a programmable logic array (PLA) into at least two sub-PLAs by avoiding unbalanced columns in an AND plane of a set of equations

representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA." This is distinguishable from Shau as Shau discloses balancing miniterms of sub-PLAs and organizing sub-PLAs after they are formed (i.e., after the PLA is split).

Moreover, Shau asserts that there are many other methods applicable to partition a large PLA into sub-PLA's, but none of the teachings of Shau disclose, teach, or suggest all the limitations contained in Applicant's amended claims 1, 10, 17, 24, 29 and 36. (See Shau, column 8, lines 32-47).

Therefore, since Shau does not disclose, teach or suggest all of Applicant's amended claims 1, 10, 17, 24, 29 and 36 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Shau. Thus, Applicant's amended claims 1, 10, 17, 24, 29 and 36 are not anticipated by Shau. Additionally, the claims that directly or indirectly depend on claims 1, 10, 17, 24, 29 and 36, namely claims 2-3 and 6-9, 11-16, 18-19 and 22-23, 25-28, 30-35, and 37-40, respectively, are also not anticipated by Shau for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(e) rejections for claims 1-3, 6-19, and 22-40 are respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-3, 6-7, 9-14, 16-19, 22, 24-27, 29-33 and 35-39 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: January 4, 2005

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on January 4, 2005.

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Jean Svoboda